IN THE CLAIMS

Please cancel claim 13.

Please amend claims 1, 7, 12, and 14 as follows:

1. (Currently Amended) A self refresh control apparatus, for use in a semiconductor memory device, comprising:

a self refresh entry unit having at least one clock buffer for generating a self refresh entry signal in response to an external control signal, wherein the clock buffer generates a clock signal in response to an external clock signal and a clock buffer enable signal;

a self refresh exit unit for generating a first self refresh exit signal in response to the external control signal and generating a second self refresh exit signal synchronized with the clock signal;

a clock buffer controller for generating the clock buffer enable signal in response to the first self refresh exit signal; and

a self refresh signal generator for generating a self refresh signal in response to the self refresh entry signal and the second self refresh exit signal, wherein the self refresh signal is fed back and input to the self refresh entry unit ~~100A.~~

2. (Original) The self refresh control apparatus as recited in claim 1, wherein the self refresh entry signal is synchronized with the external clock signal.

3. (Original) The self refresh control apparatus as recited in claim 2, wherein the second self refresh exit signal is synchronized with the external clock signal.

4. (Original) The self refresh control apparatus as recited in claim 1, wherein the self refresh entry unit includes:

a command buffer for receiving a plurality of command signals to output a plurality of internal command signals;